

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Paul A. Farrar et al.
Title: BURIED CONDUCTORS

Docket No.: 303.367US3
Filed: November 11, 2003
Examiner: Unknown
Customer No.: 21186

Serial No.: 10/705185
Due Date: N/A
Group Art Unit: Unknown
Confirmation No.:


Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

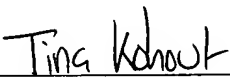
- ☒ A return postcard.
- ☒ An Supplemental Information Disclosure Statement (2 pgs.), Form 1449 (1 pg.), and copies of 7 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

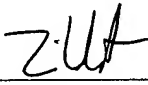
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Customer Number 21186

By: 
Atty: Timothy B. Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 1st day of December 2003.



Name



Signature

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. Customer Number 21186
(GENERAL)



10/705,185

PATENT

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Title:	BURIED CONDUCTORS		

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Supplemental Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Supplemental Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Supplemental Information Disclosure Statement considered.

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Serial No :10/705185

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Title: BURIED CONDUCTORS

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The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

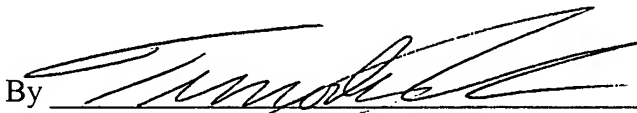
Respectfully submitted,

PAUL A. FARRAR ET AL.

By their Representatives,

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Date 1 Dec '03

By 
Timothy B Clise
Reg. No. 40,957

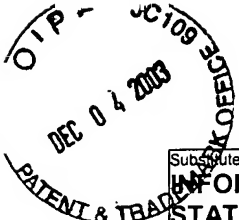
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Name

Tina Kibauk

Signature





Substitute for form 1449A/PTO
**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Use as many sheets as necessary)

Complete if Known

Application Number 10/705185

Filing Date November 11, 2003

First Named Inventor Farrar, Paul

Group Art Unit Unknown

Examiner Name Unknown

Sheet 1 of 1

Attorney Docket No: 303.367US3

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-3,932,226	01/13/1976	Klatskin, J. B., et al.	204	16	12/06/1974
	US-4,670,297	06/02/1987	Lee, K., et al.	427	91	06/21/1985
	US-4,857,481	08/15/1989	Tam, G., et al.	437	182	03/14/1989
	US-5,158,986	10/27/1992	Cha, S. W., et al.	521	82	04/05/1991
	US-5,268,315	12/07/1993	Prasad, J. S., et al.	437	31	09/04/1992
	US-5,308,440	05/03/1994	Chino, T., et al.	156	664	09/02/1992
	US-5,334,356	08/02/1994	Baldwin, D. F., et al.	422	133	08/24/1992
	US-5,539,227	07/23/1996	Nakano, H.	257	276	08/02/1995

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T ²
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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	✓	ABIDI, "Large Self-Suspended Inductors on Silicon and Their Use in 2- μ m CMOS RF Amplifier", <u>IEEE Electron Device Letters</u> , Vol. 17, No. 9, (1993),246-48	
	✓	BURGHARTZ, et al., "Integrated RF and Microwave Components in BiCMOS Technology", <u>IEEE Trans. Electron Devices</u> , Vol. 43, No. 9,(1996),1559-70	
	✓	BURGHARTZ, et al., "Multi-level Spiral Inductors Using VLSI Interconnect Technology", <u>IEEE Electron Device Letters</u> , Vol. 17, No. 9, (1996),428-30	
		JIN, C., et al., "Porous Xerogel Films as Ultra-low Permittivity Dielectrics for ULSI Interconnect Applications", <u>Conference Proceedings ULSI XII - 1997 Materials Research Society</u> , (1997),pp. 463-469	
	✓	MEYER, et al., "Si IC-Compatible Inductors and LC Passive Filters", <u>IEEE Journal of Solid State Circuits</u> , Vol. 25, No. 4, (1990),1028-31	
	✓	MILLER, R. D., et al., "Low Dielectric Constant Polyimides and Polyimide Nanofoams", <u>Seventh Meeting of the DuPont Symposium on Polyimides in Microelectronics</u> , (September 1996),pp. 443-473	
	✓	TING, C. H., "Methods and Needs for Low K Material Research", <u>Materials Research Society Symposium Proceedings</u> , Volume 381, Low-Dielectric Constant Materials -- Synthesis and Applications in Microelectronics, Lu, T.M., et al., (eds.), San Francisco, CA,(April 17-19, 1995),3-17	

EXAMINER

DATE CONSIDERED

Substitute Disclosure Statement Form (PTO-1449)

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 809. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached